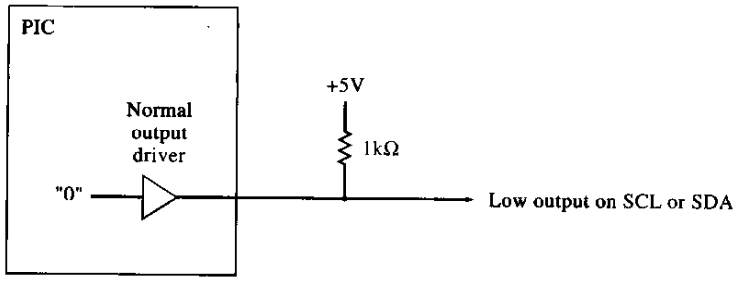
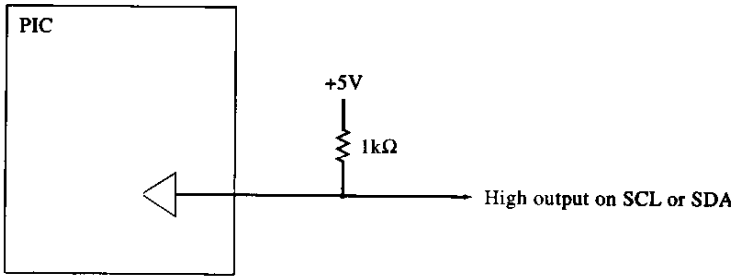


(a) I/O pin set to be an output with "0" written to it



(b) I/O pin set to be an input

Figure 9-1 Implementation of open-drain outputs.

the clock line is released by the receiver. The open-drain feature is also needed if this PIC will ever become an I^2C slave to another PIC, in which case it must relinquish control of the SCL line.

Figure 9-2 also illustrates that the first eight *data* bits on the SDA line are sent by the transmitter, whereas the ninth *acknowledge* bit is a response by the receiver. For example, when the PIC sends out a chip address, it is the transmitter, while every other chip on the I^2C bus is a receiver. During the acknowledge bit time, the *addressed* chip is the only one that drives the SDA line, pulling it low in response to the master's pulse on SCL, acknowledging the reception of its chip address.

When the byte transfer represents data being returned to the PIC from a peripheral chip, it is the peripheral chip that drives the eight data bits in response to the clock pulses from the PIC. In this case, the acknowledge bit is driven in a special way by the PIC, which is serving as receiver but also as bus master. If the peripheral chip is one that can send the contents of successive internal addresses back to the PIC (e.g., a serial EEPROM), then the PIC completes the reception of each byte and signals a request for the next byte by pulling the SDA line low in acknowledgment. After any number of bytes have been received in this way from the peripheral, the PIC can signal the peripheral to stop any further transfers by *not* pulling the SDA line low in acknowledgment.

(dri

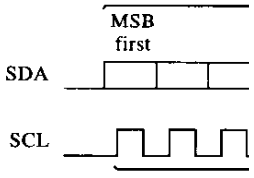


Figure 9-2 Byte transfe

Figure 9-2 also illus
of the clock. When the s
it initiates the new bit ir
that bit on the SDA line
When the PIC mast
it changes SDA after dri
it changes SCL and SD/
I^2C bus transfers c
either another START c
the SDA and the SCL li
tiates a transfer with the
in Figure 9-3a. Likewis
both SDA and SCL initi
these occurrences are e
consist of a change in t
of a byte transfer.
The PIC I^2C bus m
slave address followed
transmitted on the bus w
sequent bytes will be se
The I^2C bus standa
with what looks like a r
plus a second 8-bit addi
peripheral chips to be d
chips having an I^2C int
not be discussed here.
The functions of th
peripheral chip. For a pe
the PIC will typically wr
address. Subsequent byt
the consecutive addresse
A message string fo
begins with a 2-byte m