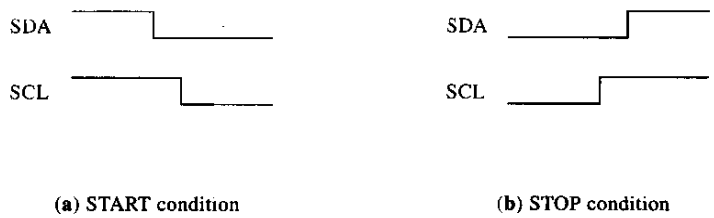


Figure 9-3 I2C START and STOP conditions.

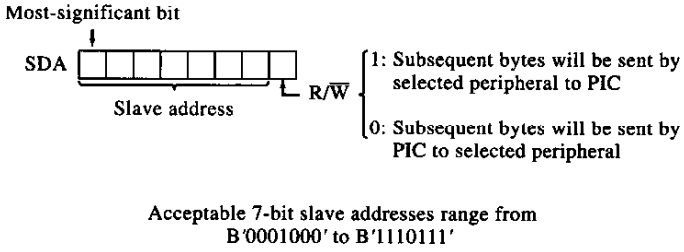


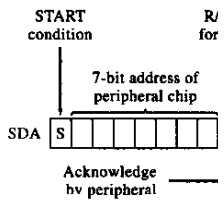
Figure 9-4 First byte of a message string.

Then a second START condition initiates a new message string. The first byte of this new message string again selects the same peripheral chip but signals that the subsequent bytes are to consist of reads from successive addresses in the peripheral chip.

The 1995 I²C bus specification includes the timing constraints for older chips designed for a maximum bit rate of 100 kbit/s. It also includes the constraints for newer *fast-mode* 400 kbit/s parts. The three chips discussed in this chapter all support 400 kbit/s transfers. The timing diagrams of Figures 9-6a through 9-6c define the timing parameters. The table of Figure 9-6d lists the worst-case values and translates these to internal clock cycles for a PIC operating at any one of three crystal frequencies. These are the values needed when code is written to generate the I²C waveforms.

9.3 I²C BUS SUBROUTINES

Because the SCL pin must have an open-drain output while the SDA pin must be either an input or have an open-drain output, the I²C bus subroutines will repeatedly access **TRISC**, the data direction register for **PORTC**. However, **TRISC** is located at the Bank 1 address, H'87', which cannot be accessed by direct addressing without first executing the instruction



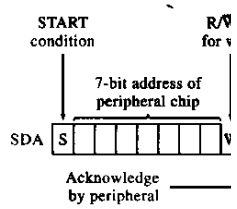


Figure 9-5 I²C typic

```
bsf
```

then changing the requi

```
bcf
```

Instead of doing this, loa
bit setting and bit cleari

```
SCL     equ
```

and

```
SDA     equ
```

then

```
bsf
```

will release the SDA lin
I²C chip pull it low.